What is claimed is:

1. A method for forming active regions of field effect transistors, comprising:

(a) forming at least one conductive region over an isolation layer formed on a substrate, and a cap dielectric layer on the at least one conductive region;

(b) forming a sacrificial dielectric layer over the isolation layer and the cap dielectric layer, and on sidewalls of the at least one conductive region;

(c) removing a portion of the sacrificial dielectric layer on the cap dielectric layer;

(d) removing the cap dielectric layer; and

(e) removing remaining portions of the sacrificial dielectric layer.

2. The method of claim 1, wherein the cap dielectric layer includes a first cap dielectric layer and a second cap dielectric layer.

3. The method of claim 2, wherein step (d) comprises the step of removing the first cap dielectric layer and the second cap dielectric layer.

4. The method of claim 3, wherein the sacrificial dielectric layer is formed to a thickness at least larger than a thickness loss caused by removing the first cap dielectric layer and the second cap dielectric layer.

5. The method of claim 1, further comprising performing a sputtering step to trim the remaining portions of the sacrificial dielectric layer prior to removal thereof.

6. The method of claim 1, wherein the at least one conductive region has a mesa structure.

7. The method of claim 1, wherein the sacrificial dielectric layer is formed to a thickness at least larger than a thickness loss caused by step (d).

8. The method of claim 1, wherein step (c) is performed by a chemical mechanical polish (CMP) process with a high selectivity slurry.

9. The method of claim 8, wherein the CMP process with the high selectivity slurry has different removing rates for different regions of the sacrificial dielectric layer in response to different polish pressures applied thereto.

10. The method of claim 9, wherein the high selectivity slurry comprises a ceria-based abrasive and an electronegative surfactant.

11. The method of claim 1, further comprising the step of performing a cleaning process after step (d), wherein said sacrificial dielectric layer has a thickness during said cleaning process sufficient to substantially protect said at least one conductive region from undercut in the isolation layer.

12. A method for forming active regions of field effect transistors, comprising:

(a) forming at least one conductive mesa over an isolation layer formed on a substrate, and a cap dielectric layer on the at least one conductive mesa;

(b) forming a sacrificial dielectric layer over the isolation layer and the cap dielectric layer, and on sidewalls of the at least one conductive mesa;

(c) removing a portion of the sacrificial dielectric layer on the cap dielectric layer by a chemical mechanical polish (CMP) process with a high selectivity slurry;

(d) removing the cap dielectric layer, wherein the sacrificial dielectric layer is formed to a thickness at least larger than a thickness loss caused by removal step (d); and

(e) removing remaining portions of the sacrificial dielectric layer.

13. The method of claim 12, wherein the cap dielectric layer includes a first cap dielectric layer and a second cap dielectric layer.

14. The method of claim 13, wherein step (d) comprises the step of removing the first cap dielectric layer and the second dielectric layer.

15. The method of claim 14, wherein the sacrificial dielectric layer is formed to a thickness at least larger than a thickness loss caused by removing the first cap dielectric layer and the second cap dielectric layer.

16. The method of claim 12, further comprising performing a sputtering step to trim the remaining portions of the sacrificial dielectric layer prior to removal thereof.

17. The method of claim 12, wherein the CMP process with the high selectivity slurry has different removing rates for different regions of the sacrificial dielectric layer in response to different polish pressures applied thereto.

18. The method of claim 17, wherein the high selectivity slurry comprises a ceria-based abrasive and an electronegative surfactant.

19. A method for forming field effect transistors, comprising:

(a) forming at least one conductive mesa over an isolation layer formed on a substrate, and a cap dielectric layer on the at least one conductive mesa;

(b) forming a sacrificial dielectric layer over the isolation layer and the cap dielectric layer, and on sidewalls of the at least one conductive mesa;

(c) removing a portion of the sacrificial dielectric layer on the cap dielectric layer by a chemical mechanical polish (CMP) process with a high selectivity slurry;

(d) removing the cap dielectric layer;

(e) removing remaining portions of the sacrificial dielectric layer;

(f) forming a gate on the at least one conductive region; and

(g) forming source/drain (S/D) regions within the at least one conductive region and adjacent to the gate.

20. The method of claim 19, wherein the cap dielectric layer includes a first cap dielectric layer and a second cap dielectric layer.

21. The method of claim 20, wherein step (d) comprises the step of removing the first cap dielectric layer and the second dielectric layer.

22. The method of claim 21, wherein the sacrificial dielectric layer is formed to a thickness at least larger than a thickness loss caused by removing the first cap dielectric layer and the second cap dielectric layer.

23. The method of claim 19, further comprising performing a sputtering step to trim the remaining portions of the sacrificial dielectric layer prior to removal thereof.

24. The method of claim 19, wherein the at least one conductive region has a mesa structure.

25. The method of claim 19, wherein the sacrificial dielectric layer is formed to a thickness at least larger than a thickness loss caused by step (d).

26. The method of claim 19, wherein step (c) is performed by a chemical mechanical polish (CMP) process with a high selectivity slurry.

27. The method of claim 26, wherein the CMP process with the high selectivity slurry has different removing rates for different regions of the sacrificial dielectric layer in response to different polish pressures applied thereto.

28. The method of claim 27, wherein the high selectivity slurry comprises a ceria-based abrasive and an electronegative surfactant.

29. An integrated circuit including a field effect transistor, the field effect transistor comprising:

a conductive region on a substrate having an isolation layer formed thereon, the isolation layer being substantially without undercut at the region within the isolation layer beneath the conductive region;

a gate on the conductive region; and

source/drain (S/D) regions within the conductive region and adjacent to the gate.

30. The integrated circuit of claim 29, wherein any undercut within the isolation layer beneath the conductive region has a lateral depth no more than about 100Å.

31. The integrated circuit of claim 29, wherein the conductive region has a mesa structure.

32. An integrated circuit including a plurality field effect transistors having active regions formed by the process of claim 1.

33. A method for forming field effect transistors, comprising:

(a) forming at least one conductive region over an isolation layer formed on a substrate;

(b) forming a sacrificial dielectric layer over the isolation layer and adjacent to said at least one conductive region;

(c) forming a gate dielectric layer over said at least one conductive region, and

(d) performing a cleaning process prior to forming said gate dielectric layer, wherein said sacrificial dielectric layer is formed to a thickness sufficient to substantially protect said at least one conductive region from undercut in the isolation layer from said cleaning process.

34. The method of claim 33, wherein said cleaning process utilizes a HF solution.